Graphene Barristor, a Triode Device with a Gate-Controlled Schottky Barrier

Heejun Yang, Jinsong Heo, Seongjun Park, Hyun Jae Song, David H. Seo, Kyung-Eun Byun, Philip Kim, InKyeong Yoo, Hyun-Jong Chung, Kinam Kim

Despite several years of research into graphene electronics, sufficient on/off current ratio \( I_{\text{on}}/I_{\text{off}} \) in graphene transistors with conventional device structures has been impossible to obtain. We report on a three-terminal active device, a graphene variable-barrier "barristor" (GB), in which the key is an atomically sharp interface between graphene and hydrogenated silicon. Large modulation on the device current (on/off ratio of \( 10^5 \)) is achieved by adjusting the gate voltage to control the graphene-silicon Schottky barrier. The absence of Fermi-level pinning at the interface allows the barrier’s height to be tuned to 0.2 electron volt by adjusting graphene’s work function, which results in large shifts of diode threshold voltages. Fabricating GBs on respective 150-mm wafers and combining complementary p- and n-type GBs, we demonstrate inverter and half-adder logic circuits.

The triode, composed of a diode and a grid in a vacuum tube, was the first three-terminal active device that had been used to amplify and to switch electric signals, which led to the technical innovations for modern electronics in the early 20th century (1). Solid-state transistors and integrated circuits (ICs) based on silicon were more practical for complicated logic circuits and thus replaced triodes. Although silicon transistors have continued to improve their speed and integration density, they now near the potential limit where further reduction of channel length causes inevitable leakage currents (2). To present an alternative route for overcoming these challenges, we introduce a class of three-terminal devices based on a graphene-silicon hybrid device that mimics a triode operation. The key device function takes place at the electrostatically gated graphene/silicon interface where a tunable Schottky barrier controls charge transport across a vertically stacked structure. We named this barrier variable device, which is a solid-state descendant of the triode, “barristor.”

Graphene is a zero-gap semiconductor whose Fermi energy can be adjusted by electrostatic gating owing to its two-dimensional (2D) nature (3–5). Because graphene is metallic at a sufficiently large Fermi energy, a Schottky barrier (SB) forms at the interface between the doped graphene and the semiconductor (6–10). However, SB between graphene and a well-controlled semiconductor surface, such as hydrogen-terminated Si, is different from a conventional metal-semiconductor SB in two important ways. First, the formation of interface states is suppressed in graphene-semiconductor junctions (11) because the interaction between chemically inert graphene and a completely saturated semiconductor surface—that is, one without dangling bonds—is negligible (12). Second, graphene’s work function (WF) can be adjusted electrostatically over a wide range by tuning the Fermi energy (\( E_F \)) via the electrostatic field effect (13, 14). We could realize a graphene barristor (GB) by combining these two effects, as also shown in (15).

A schematic diagram of the GB structure and its top view are shown in Fig. 1, A and B. Single-layer graphene in contact with the source electrode forms the SB at its interface with the silicon surface at the drain contact. Two kinds of GBs can be formed depending on the silicon doping type: n-type GB at n-type silicon and p-type GB at p-type silicon. We used transmission electron microscopy (TEM) to develop an optimal transfer process for graphene onto Si substrates to create atomically sharp interfaces (inset of Fig. 1C), which minimizes atomic defects or silicon dioxide formation that can create charge trapping sites. Figure 1C displays a typical Schottky diode characteristic of a p-type GB with an optimized graphene/Si interface. The forward characteristic at a low bias showed a diode ideality factor \( \eta_d \approx 1.1 \) for this particular device. The ideality factor we obtained in our GB is considerably better than those reported in exfoliated graphene-Si junctions (9), confirming the high interfacial quality in our GBs.

The recent availability of large-scale graphene growth through chemical vapor deposition (CVD) techniques (16–20) allowed us to integrate graphene devices at wafer scales using conventional semiconductor microfabrication processes (21). Large-scale integration has not been possible for similar devices such as p-n diodes demonstrated in highly customized and suspended semiconducting

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Fig. 1. Graphene barristor. (A) A schematic diagram to show the concept of a GB. (B) False-colored scanning electron microscope image of the GB before the top gate fabrication process. (C) Current versus bias voltage characteristic of a GB at a fixed gate voltage \( V_{\text{gate}} = 0 \text{ V} \), showing a Schottky diode characteristic. The inset shows a TEM image of graphene/silicon junction. No native oxide or defect is seen in the image. (D) A photograph of ~2000 GB arrays implemented on a 6-inch wafer.
Fig. 2. Graphene barristor characteristics. The current and bias voltage characteristics of p-type (main panel) and n-type (inset) GBs at various fixed $V_{\text{gate}}$ values. $V_{\text{gate}}$ varies in the range $-5$ to $5$ V, with a step size of 1 V for each curve. The red arrow indicates the direction of increasing $V_{\text{gate}}$.

Fig. 3. (A) Temperature-dependent diode characteristic. The saturation current of the n-type GB, $I_{\text{sat}}$, is obtained by measuring the current at $V_{\text{bias}} = 2.5$ V at various temperature and gate voltage values. Different colors are used for different $V_{\text{gate}}$ from $-1$ to $4$ V with $1$- to $2$-V step variation. The line fit for each $V_{\text{gate}}$ value is drawn to yield the Schottky barrier height from the slope of the fitted line. (B) The Fermi energy on the right $y$ axis is obtained from Hall measurement at the same gate voltage $V_{\text{gate}}$. Monotonic increase and decrease of observed SB height is consistent with the band diagrams in (C) and (D), respectively. (C and D) Schematic band diagrams of GB with the EFE generated by the gate on the top of graphene. Applying negative voltage on the gate induces holes in graphene, increasing its work function and increasing the Schottky barrier height. As a result, the reverse current across the Schottky barrier decreases (C). Positive gate voltage decreases the Schottky barrier height and increases reversed current (D).

The current and bias voltage characteristics of p-type (main panel) and n-type (inset) GBs at various fixed $V_{\text{gate}}$ values. $V_{\text{gate}}$ varies in the range $-5$ to $5$ V, with a step size of 1 V for each curve. The red arrow indicates the direction of increasing $V_{\text{gate}}$. Figure 2D shows the graphene barristor characteristics. The saturation current of the n-type GB, $I_{\text{sat}}$, is obtained by measuring the current at $V_{\text{bias}} = 2.5$ V at various temperature and gate voltage values. Different colors are used for different $V_{\text{gate}}$ from $-1$ to $4$ V with $1$- to $2$-V step variation. The line fit for each $V_{\text{gate}}$ value is drawn to yield the Schottky barrier height from the slope of the fitted line. (B) The Fermi energy on the right $y$ axis is obtained from Hall measurement at the same gate voltage $V_{\text{gate}}$. Monotonic increase and decrease of observed SB height is consistent with the band diagrams in (C) and (D), respectively. (C and D) Schematic band diagrams of GB with the EFE generated by the gate on the top of graphene. Applying negative voltage on the gate induces holes in graphene, increasing its work function and increasing the Schottky barrier height. As a result, the reverse current across the Schottky barrier decreases (C). Positive gate voltage decreases the Schottky barrier height and increases reversed current (D).

$V_{\text{bias}} = 25$ V

$\ln(I_{\text{sat}})/T^2$ vs. $1/(kT)$ for various $V_{\text{gate}}$: -1 V, 1 V, 2 V, and 4 V.

$\Delta E_F$ vs. $V_{\text{gate}}$ for various $V_{\text{bias}}$: 0.16 eV, 0.12 eV, and 0.08 eV.

$\phi_b$ at various $V_{\text{gate}}$: -5 V to 5 V, with a step size of 1 V for each curve.

The saturation current of the n-type GB, $I_{\text{sat}}$, is obtained by measuring the current at $V_{\text{bias}} = 2.5$ V at various temperature and gate voltage values. Different colors are used for different $V_{\text{gate}}$ from $-1$ to $4$ V with $1$- to $2$-V step variation. The line fit for each $V_{\text{gate}}$ value is drawn to yield the Schottky barrier height from the slope of the fitted line. (B) The Fermi energy on the right $y$ axis is obtained from Hall measurement at the same gate voltage $V_{\text{gate}}$. Monotonic increase and decrease of observed SB height is consistent with the band diagrams in (C) and (D), respectively. (C and D) Schematic band diagrams of GB with the EFE generated by the gate on the top of graphene. Applying negative voltage on the gate induces holes in graphene, increasing its work function and increasing the Schottky barrier height. As a result, the reverse current across the Schottky barrier decreases (C). Positive gate voltage decreases the Schottky barrier height and increases reversed current (D).

We could electrostatically modulate the graphene’s WF through the top gate electrode and gate dielectric above the graphene (14), which resulted in a variation on the SB height. Because the injection of the majority carriers from graphene to silicon is determined by the SB height $\phi_b$, the top gate then directly controls the magnitude of the current across the source and the drain. The main panel of Fig. 2 shows the characteristic of p-type GB at various gate voltages ($V_{\text{gate}}$). The rectification behavior of the GB was demonstrated in that the GB current ($I_{\text{sat}}$) increased steeply as the bias voltage ($V_{\text{bias}}$) surpassed the “turn-on” voltage, $V_{\text{TO}}$. $V_{\text{TO}}$ could be adjusted between 0 V and 1.3 V as $V_{\text{gate}}$ was modulated between $-5$ and $5$ V, the range needed to keep this GB in p-type operation. Similar triode behavior was observed in n-type GBs (Fig. 2 inset), where the bias polarity was reversed because electrons become the majority carrier. The large modulation of the GB current was indicative of a large variation in the SB height, caused by the electric field effect (EFE) from $V_{\text{gate}}$.

To quantitatively analyze the device characteristic, we used the diode equation

$$I = A^* A^* T^2 \exp \left( -\frac{q\phi_b}{kT} \right) \left[ \exp \left( \frac{qV_{\text{bias}}}{n_kT} \right) - 1 \right]$$

where $A$ is the area of the Schottky junction, $A^*$ is the effective Richardson constant, $q$ is the elementary charge, $k_T$ is the Boltzmann constant, and $T$ is the temperature. Quantitative analysis of the SB height $\phi_b$ can be done by investigating the temperature dependence of the GB current in the reverse bias saturation regime [$\exp(qV_{\text{bias}}/n_kT) < 1$]. Here, the diode current becomes insensitive to $V_{\text{bias}}$ and $I_{\text{sat}} \propto T^2 \exp \left( \frac{q\phi_b}{kT} \right)$. Figure 3A shows a plot of $\ln(I_{\text{sat}})/T^2$ vs. $1/(kT)$ in the reverse bias saturation regime. We estimated the SB height $\phi_b$ for a given gate voltage $V_{\text{gate}}$ from the slope of each curve. Figure 3B shows the resulting SB heights obtained as a function of $V_{\text{gate}}$. $V_{\text{gate}}$ increased from 0 to 5 V, and $\phi_b$ decreased substantially from 0.45 eV to 0.25 eV. We attributed the drastic change in $\phi_b$ to the EFE-induced Fermi level change, $\Delta E_F$. Indeed, as shown in Fig. 3B, the measured variation of $\phi_b$, $\Delta \phi_b =$...
φ = φ₀(ΔEF = 0), was well correlated to the change of ΔEF, obtained independently by calculating the measured Hall carrier density (nH) using ΔEF = hνF/σνH, where vF = 10⁶ m/sec was used for the Fermi velocity of graphene. We observed that ΔDB ≈ −ΔEF for a wide range of Vgate (Fig. S7), which suggests that the WF modulation of graphene in the absence of Fermi-level pinning is fully responsible for the variation of φ₀ as depicted in Fig. 3, C and D.

The absence of Fermi-level pinning, one of the major sources for high device resistance in silicon electronics (26), comes from the suppression of the surface states at the interface of silicon and graphene. In our GB, we could eliminate the “Fermi-level pinning” and manipulate the SB height as in the ideal Schottky-Mott limit (Fig. 3B), where the SB height is controlled through the selection of metal and semiconductor with appropriate WFs (27, 28).

Two different types of GB operations are possible, as shown in Fig. 4A. The first type uses the GB in the reverse-biased regime (orange shaded region in Fig. 4A). Here, a conventional FET-like device operation could be possible; that is, the GB current, I, had the tendency to saturate at large reverse bias voltages, and the on-state current, Ion, had been modulated by Vgate. The off-state current, Ioff, was determined at the highest achieved SB, which yielded an Ion/Ioff ratio of ~300 in Fig. 4A. The second type of operation could be realized by using the device in the forward biasing region (the blue shaded region in Fig. 4A). In this regime, the diode current did not saturate as Vbias increased but deviated from a typical FET-like device operation. However, near the diode turn-on regime, I varied by several orders of magnitude as Vgate changed, resulting in a switching operation with a large Ion/Ioff ratio. Figure 4B shows the switching characteristic of the diode current in the forward-biased p-type GB, demonstrating a high Ion/Ioff ratio of ~10⁵. We note that the large Ion/Ioff ratio and small off-state current overcame the key obstacle in graphene-based electronics.

Three-terminal operation of GB offers various integrated device functionalities. Similar to the complementary metal-oxide semiconductor inverter operation, a series connection of n- and p-type complimentary GBs inverted the input signal Vin to its inverse Vout (Fig. 4C). The low Vout originated from the high on/off current ratio of GBs, which implies that only a small amount of static off-state power would be consumed. As for more complicated logic applications, we demonstrated a half-adder circuit built from n- and p-type 10 GBs. The schematic with two inputs (A and B) and two outputs (SUM and CARRY) is shown in Fig. 4D. The measured output voltage levels are represented in Fig. 4E. These results suggest that the GB can provide a route to realize high-speed logic applications (29, 30) based on graphene-semiconductor hybrid devices.

In conclusion, our GB suggests the possibility of a graphene logic device by achieving a high on/off ratio of ~10⁵, which exceeds the minimum requirement for logic transistors. Furthermore, the on/off ratio and the current density can be improved with well-developed semiconductor processes because there is not a fundamental (or structural) limit. GB also has an advantage in lateral scaling because the barrier is formed vertically.

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21. Materials and methods are available as supplementary materials on Science Online.
Tailoring Electrical Transport Across Grain Boundaries in Polycrystalline Graphene

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Graphene produced by chemical vapor deposition (CVD) is polycrystalline, and scattering of charge carriers at grain boundaries (GBs) could degrade its performance relative to exfoliated, single-crystal graphene. However, the electrical properties of GBs have so far been addressed indirectly without simultaneous knowledge of their locations and structures. We present electrical measurements on individual GBs in CVD graphene first imaged by transmission electron microscopy. Unexpectedly, the electrical conductance improves by one order of magnitude for GBs with better interdomain connectivity. Our study suggests that polycrystalline graphene with good stitching may allow for uniformly high electrical performance rivaling that of exfoliated samples, which we demonstrate using optimized growth conditions and device geometry.

In Fig. 1A, we show false-color dark-field TEM (DF-TEM) images of graphene films grown under three different conditions [see supplementary materials (13)] taken in a manner similar to Huang et al. (4). Each colored region corresponds to a separate graphene crystalline domain with distinct lattice orientation. The image is generated by using an aperture in the back-focal plane of the microscope to collect electrons diffracted from only a narrow range of angles by the graphene lattice. In general, different graphene domains produce a diffraction pattern rotated with respect to one another, so each domain can be imaged separately, colorized, and then combined.

In growth A, graphene was synthesized under high reactant flow rates, which produced fast growth and also small average domain size $D \approx 1 \mu m$. Graphene from growth B was synthesized in a diluted methane environment, whereas growth C was further enclosed in copper foil, after Yu et al. (14), resulting in slower growths. The latter films were terminated after only partial surface coverage to highlight their growth structures. In subsequent microscopy and electrical measurements, however, we used continuous films, for which growth B yielded $D \approx 10 \mu m$ and growth C, $D \approx 50 \mu m$. The overall shapes of partially grown graphene islands in growth B were polygons, whereas growth C generally formed flowered islands (fig. S1). Despite

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Fig. 1. (A) Composite false-color DF-TEM images of CVD graphene produced using three different growth conditions—A, B, and C—yielding average domain size $D$ of 1, 10, and 50 $\mu m$, respectively, in continuous films. (B) (Left) Schematic of specially fabricated TEM chip compatible with electron-beam lithography and electrical measurements. (Top right) SEM image of top-gated, graphene Hall bar device. (Bottom right) Overlaid SEM and DF-TEM images showing device crossing a single GB of two domains from growth C. Scale bars, 1 $\mu m$. 

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Materials and Methods

Supplementary Text
Figs. S1 to S10

References
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**Materials and Methods**

**Preparation of Graphene-Silicon Junction**

A single layer graphene-silicon junction is formed by transferring CVD-grown graphene onto pre-patterned Si substrates. The pre-patterning was conducted on a 100 nm thick SiO$_2$ layer grown on a 6 inch wafer of n-Si (doping density of $\sim 10^{16}$ cm$^{-3}$) or p-Si (doping density of $\sim 10^{17}$ cm$^{-3}$). Using photolithography and Buffered Oxide Etch (BOE) processes, windows exposing bare Si underneath were fabricated with the dimension, 2 $\mu$m $\times$ 4 $\mu$m. Before transferring graphene, native oxide on the exposed Si substrate was carefully removed by additional wet etching followed by the passivation of Si surface with hydrogen treatment in a controlled atmosphere. After placing the graphene on the substrate, Raman spectrum was obtained to determine the quality of transferred graphene. Fig. S1 shows Raman spectrum of graphene on SiO$_2$ and graphene on Si. Well-developed G ($\sim 1600$ cm$^{-1}$) and 2D ($\sim 2700$ cm$^{-1}$) peaks with no appreciable increase of D peak ($\sim 1300$ cm$^{-1}$) indicate that the single layer graphene is well maintained on both SiO$_2$ and Si after the wafer-scale transfer process.

**Supplementary Text**

**Device Uniformity on 6 Inch Wafer**

Fig. S2A shows a histogram of mobility for graphene devices measured in field effect transistor (FET) operation mode on the 6 inch wafers. Around 2000 FET devices were fabricated and measured on the wafer. More than 90% of the devices showed proper field
effect mobility and the measured average mobility was around 1300 cm$^2$/V·s. A few representative device characteristics are shown in Fig. S2B.

The Ideality Factor and Diode On-Current Density

Similar to the p-type Schottky diode operation demonstrated in Fig. 1C, we also demonstrate an ideality factor of up to 1.1 in n-type Schottky diode operation (Fig. S3). This value is the best ideality factor reported in graphene Schottky junctions, reflecting the high quality of interface we achieved between graphene/Si.

While the ideality factor of a graphene barrister (GB) device is determined by the interface quality between the graphene and Si channel, the saturation on-current density is subject to a series resistance, composed of the sheet resistance of graphene and the resistance of a reverse biased Schottky junction at the interface between ‘Drain electrode’ and silicon. Those two resistances can be improved by shaping graphene to having lower sheet resistance and high concentration doping to to lower the Schottky resistance.

Given that we use forward bias current of graphene/silicon Schottky junction, there are two critical reasons for the current density limits: graphene-metal contact resistance (graphene-Au in our case) and reverse Schottky regime of the opposite electrode (silicon and drain electrode). Eventually, graphene-metal contact resistance will also limit the maximum saturation current in our GBs. Fig. S4 shows a device where some parts of such optimizations are implemented. In this device, operation current density up to 5x10$^3$ A/cm$^2$ is achieved, more than two orders of magnitude improvement compared to un-optimized devices. Further
improvement of device architecture and doping of the Metal-Si contacts will further increase the attainable saturation current density.

We also note that although our work is for realizing new idea toward graphene-based electronics at this stage, our device already meets the current density specification of some applications. For example, thin film transistor (TFT) requires an on-current of 1~10 μA, or an on-current density of 1~10 A/cm² (24). Since the graphene mobility is far beyond the current TFT material, there could be a breakthrough in such applications.

**Transmission Electron Microscopy Analysis**

We analyze the quality of the graphene/Si interface using cross sectional imaging of the junction using TEM. The well-optimized transfer process we developed produce atomically clean interfaces between graphene and Si free from native oxide or other contamination layers as shown in Fig.1C inset and Fig. S5B. However, we do also observe an occasional contamination in between graphene and Si interface. Fig. S5A, shows a larger area TEM image taken from un-optimized graphene transfer on Si substrate. Several regions where extra material is located between graphene and silicon (red rectangle) can be seen in this poor quality sample. We note that this extra material reduces the local thermionic emission current and degrades the ideality factors of GBs. Reducing damage on silicon substrate during the wet-etching process of silicon oxide was identified as a key in producing atomically clean interfaces.
Formula for Saturation Current in Schottky Diode

In the thermionic emission regime, the saturation current, \( I_S \) in \( I-V \) characteristic of the junction can be expressed by,

\[
I_S = A^* T^2 \exp \left( \frac{-\Phi_B}{k_B T} \right)
\]

where \( A \) is the contact area, \( A^* \) is the effective Richardson constant \( \approx 252 \text{A cm}^{-2} \text{K}^{-2} \) for n-type silicon, \( T \) is the absolute temperature, \( \Phi_B \) is the Schottky barrier height, \( k \) is the Boltzmann constant. Thus, from the current data with various temperatures (see Fig. S6), we were able to extract the barrier height, 0.407 eV at zero top gate voltage. This value is close to 0.45 eV, the energy difference value between the work function of graphene (4.5 eV) and the electron affinity of silicon, \( \chi \) (4.05 eV) and also is comparable to 0.41 eV a value close to the reported value for graphene and n-type Si (9).

Schottky Barrier (SB) versus Fermi Energy

Graphene Fermi level is modulated by top gating and the electric field effect induced carrier density can be probed by using Hall measurement. Fig. S7 inset shows the Hall resistivity (left axis) and corresponding carrier density (right axis) as a function of the top gate voltage. The Fermi energy of graphene can then be estimated from \( \Delta E_F = h \nu_F \sqrt{3m} \). Using this result, we plot in Fig. S7 the SB height versus \( \Delta E_F \). We note that \( \Delta E_F \approx \Delta \Phi_B \) in this graph, implying that the interfacial pinning is negligible.
**Temperature Endurance**

The principle GB device operation relies on the variable SB to modulate current. In the off-state, thermionic emission across the SB dominates transport while near-Ohmic transport takes place in the on-state. As shown in Fig. S8, the on-state current hardly changes under temperature variation while the off-state current increase exponentially as temperature increases. Therefore, the on/off current ratio drastically changes by temperature. Such temperature dependence of the on/off ratio variation is very common in semiconductor devices. In CMOS, with similarly sized barriers, a silicon channel shows similar temperature dependence of off-state current. Therefore, it is considered that the temperature endurance of our device would be analogous to conventional CMOS and could be overcome.

**Device Modeling of Graphene Barristor**

In order to quantitatively understand the GB device operation, we model GB with three capacitors: top gate dielectric, silicon depletion region, graphene quantum capacitance (Fig. S9). These three capacitors are involved in the device operation in terms of charge balance in a static model. The following three equations describe the above three capacitances.

Silicon: \( C_{Si} = \frac{e\varepsilon_0\varepsilon_r N_D}{\sqrt{2(V_{bi} - V_0 + V_{si} - k_B T / e)}} \) [Fem\(^{-2}\)] = \( \frac{\varepsilon_0\varepsilon_r}{W} \), \( \frac{Q}{A} = N_D W \)

Top gate dielectric: \( C_T / e = \varepsilon \frac{5}{d} \times 10^{12} \text{[cm}^{-2}\text{V}^{-1}] \)

Graphene quantum capacitance: \( C_Q = e^2 \frac{dn}{dE} = \frac{2e^2 |n_f|}{\hbar v_F \sqrt{\pi}} = \frac{2e^3 V}{\pi (\hbar v_F)^2} \)
With these formulas, we obtain an expression of electric potential at the interface of graphene and silicon. Based on these potential values and diode equation, we then compute the device current versus gate voltage. The resulting current is shown as a red curve in Fig. S10.

The dotted line is ideal device performance based on gate-induced ‘Fermi-level shifting’ in silicon. With the same gate dielectric dimension, our GB model shows steeper gate dependence than the performance of state-of-art CMOS transistor with 28 nm gate length.
Figure captions

Figure S1 | Raman spectrum of graphene on SiO2 and graphene on Si.

Figure S2 | (A) Histogram of mobility for devices on a 6 inch wafer (2000 devices in total). (B) a few example of the representative FET characteristics.

Figure S3 | Current versus bias voltage characteristic of a n-type graphene barristor at a fixed gate voltage, $V_g = 0$ V, showing a Schottky diode characteristic. Ideality factor of the diode operation, $\eta_{id} \approx 1.1$ is obtained from the line fitting in the forward bias regime (solid line).

Figure S4 | Left panel displays I-V characteristic of GB in diode operation with various fixed gate voltages in linear scale. The right panel shows the resulting diode current density showing maximum saturation current density $5 \times 10^3$ A/cm$^2$ is achieved at the forward bias regime.

Figure S5 | Transmission Electron Microscopy images of graphene/silicon, (A) defected interface showing poor interfacial quality, (B) Atomically sharp interface between graphene on Si after optimized transferring process.

Figure S6 | Temperature dependent I-V curves of graphene-silicon (p-type) diode.

Figure S7 | Schottky barrier versus graphene Fermi energy. Schottky barrier height is modulated by $\Delta \Phi_B = S \Delta E_F$, where line fitting (dotted line) gives $S \sim 1$. Inset; Hall resistivity, $\rho_{xy}$ (left axis) is measured and $n_H$ (right axis) is estimated from $n_H = B/\rho_{xy}$, where $B = 2$ T is applied magnetic field. Fermi level of graphene is then calculated by using $\Delta E_F = \hbar v_F \sqrt{m_H}$. 

Figure S8 | Temperature dependence of on- and off-state current of GB.
**Figure S9** | Schematic diagram for GB with three capacitors.

**Figure S10** | Simulation and comparison of device current (CMOS and Graphene Barristor) at room temperature.
Fig. S1
Fig. S2
Fig. S3
Fig. S4
Fig. S5
Fig. S6
$S \sim 1$

Fig. S7
$I_{\text{off}} \approx \exp(-\Phi_B/kT)$

$\Phi_B \sim 0.5$ eV

$I_{\text{on}} \sim$ nearly ohmic

Fig. S8
Fig. S9
Fig. S10

- $N_D = 10^{16}$ cm$^{-3}$
- $V_{bi} = 0.45$-$0.2$ eV (built-in potential)
- $\varepsilon_s = 12$ (silicon)
- Gate thickness $d = 0.6$ nm, $\varepsilon = 4$ (SiO$_2$)
- Area = 0.006 $\mu$m$^2$
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20. Materials and methods are available as supplementary materials on *Science* Online.


