Graphene Barristor, a Triode Device with a Gate-Controlled Schottky Barrier

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Despite several years of research into graphene electronics, sufficient $I_{on}/I_{off}$ in graphene transistors with conventional device structures has been impossible to obtain. We report on a three-terminal active device, a graphene variable-barrier “barristor” (GB), where the key is an atomically sharp interface between graphene and hydrogenated silicon. Large modulation on the device current (on/off ratio of $10^5$) is achieved by adjusting the gate voltage to control the graphene-silicon Schottky barrier. The absence of Fermi-level pinning at the interface allows the barrier’s height to be tuned to 0.2 electron volts by adjusting graphene’s work function, which results in large shifts of diode threshold voltages. Fabricating GBs on respective 150-mm wafers and combining complementary p- and n-type GBs, we demonstrate inverter and half-adder logic circuits.

The triode, composed of a diode and a grid in a vacuum tube, was the first three-terminal active device that had been used to amplify and to switch electric signals, which led the technical innovations for modern electronics in the early 20th century (1). Solid-state transistors and integrated circuits (ICs) based on silicon were more practical for complicated logic circuits and thus replaced triodes. Although silicon transistors have continued to improve their speed and integration density, they now near the potential limit where further reduction of channel length causes inevitable leakage currents (2). In order to present an alternative route for overcoming these challenges, we introduce a class of three-terminal device based on a graphene-silicon hybrid device that mimics a triode operation. The key device function takes place at the electrostatically gated graphene/silicon interface where a tunable Schottky barrier controls charge transport across a vertically stacked structure. We named this barrier variable device, which is a solid-state descendant of the triode, “barristor.”

Graphene is a zero-gap semiconductor whose Fermi energy can be adjusted by electrostatic gating owing to its two-dimensional (2D) nature (3–5). Because graphene is metallic at a sufficiently large Fermi energy, a Schottky barrier (SB) forms at the interface between the doped graphene and the semiconductor (6–10). However, SB between graphene and a well-controlled semiconductor surface, such as hydrogen-terminated Si, is different from a conventional metal-semiconductor SB in two important ways. First, the formation of interface states is suppressed in graphene-semiconductor junctions (11) because the interaction between chemically inert graphene and a completely saturated semiconductor surface i.e., without dangling bonds is negligible (12). Second, graphene’s work function (WF) can be adjusted electrostatically over a wide range by tuning the Fermi energy ($E_F$) via the electrostatic field effect (13, 14). We could realize a graphene barristor (GB) by combining these two effects.

A schematic diagram of the GB structure and its top view are shown in Fig. 1, A and B. Single-layer graphene in contact with the source electrode forms the SB at its interface with the silicon surface at the drain contact. Two kinds of GBs can be formed depending on the silicon surface doping type: n-type GB at n-type silicon and p-type GB at p-type silicon. We used transmission electron microscopy (TEM) to develop an optimal transfer process for graphene onto Si substrates in order to create atomically sharp interfaces (inset of Fig. 1C) which minimizes atomic defects or silicon dioxide formation that can create charge trapping sites. Figure 1C displays a typical Schottky diode characteristic of a p-type GB with an optimized graphene/Si interface. The forward characteristic at a low bias showed a diode ideality factor $\eta \approx 1.1$ for this particular device. The ideality factor we obtained in our GB is considerably better than those reported in exfoliated graphene-Si junctions (9), confirming the high interfacial quality in our GBs.

The recent availability of large-scale graphene growth through chemical vapor deposition (CVD) techniques (15–19) allowed us to integrate graphene devices at wafer scales using conventional semiconductor microfabrication processes (20). Large-scale integration has not been possible for similar devices such as p-n diodes demonstrated in highly customized and suspended semiconductor nanotubes (21, 22). We demonstrated integration of gate-tunable GB arrays on a 6 inch wafer by transferring a single-layer graphene grown by CVD (19, 23) onto a patterned Si substrate. Figure 1D shows an array of 2,000 devices on a 6-inch (150-mm) wafer. At room temperature, the range of the ideality factor and the current density of GBs are found to be 1.1–4.0 and $10^{1}–10^{2}$ A/cm² respectively (see figs. S3 to S5 in the supplementary materials) (24), where the variation is due to the different wafer batches. These GB devices exhibited greater than 90% device yield with excellent uniformity in terms of device characteristics across the wafer with appropriate current level (fig. S2).

We could electrostatically modulate the graphene’s WF through the top gate electrode and gate dielectric above the graphene (14), which resulted in a variation on the SB height. Because the injection of the majority carriers from graphene to silicon is determined by the SB height $\varphi_s$, the top gate then directly controls the magnitude of the current across the source and the drain. The main panel of Fig. 2 shows the characteristic of p-type GB at various gate voltages ($V_{gate}$). The rectification behavior of the GB was demonstrated in that the GB current ($I_{GB}$) increased steeply as the bias voltage ($V_{bias}$) surpassed the “turn-on” voltage, $V_{TO}$. $V_{TO}$ could be adjusted between 0 V and 1.3 V as $V_{gate}$ was modulated between -5 V and 5 V, the range needed to keep this GB in p-type operation. Similar triode behavior was observed in n-type GBs (Fig. 2 inset), where the bias polarity was reversed because electrons become the majority carrier. The large modulation of the GB current was indicative of a large variation in the SB height, caused by the electric field effect (EFE) from $V_{gate}$.

In order to quantitatively analyze the device characteristic, we used
The diode equation

\[ I = A A^* T^2 \exp\left(-\frac{q\phi_b}{k_B T}\right) \left[ \exp\left(\frac{qV_{bias}}{\eta B k_B T}\right) - 1 \right] \]

where \( A \) is the area of the Schottky junction, \( A^* \) is the effective Richardson constant, \( q \) is the elementary charge, \( k_B \) is the Boltzmann constant, and \( T \) is the temperature. Quantitative analysis of the SB height \( \phi_b \) can be done by investigating the temperature dependence of the GB current in the reverse bias saturation regime \( \exp(q V_{bias} / \eta B k_B T) \ll 1 \). Here, the diode current becomes insensitive to \( V_{bias} \) and \( I_{bias} \propto \exp(-q\phi_b/k_B T) \). Figure 3A shows a plot of \( \ln(I_{bias}/T^2) \) vs. \( q/k_B T \) in the reverse bias saturation regime. We estimated the SB height \( \phi_b \) for a given gate voltage \( V_{gate} \) from the slope of each curve. Figure 3B shows the resulting SB heights obtained as a function of \( V_{gate} \). Figure 3C and 3D shows the switching characteristic of the diode current in a forward biasing region (the blue shaded region in Fig. 4A). Here, a conventional FET-like device operation could be realized by using the device in the forward biasing region (the blue shaded region in Fig. 4A). In this regime, the diode current did not saturate as \( V_{bias} \) increased, but deviated from the ideal FET-like device operation. However, near the diode turn-on regime, \( I \) varied by several orders of magnitude as \( V_{bias} \) increased, resulting in a switching operation with a large \( I_{on}/I_{off} \) ratio. Figure 4B shows the switching characteristic of the diode current in a forward biased p-type GB, demonstrating a remarkably high \( I_{on}/I_{off} \) ratio. We note that the large \( I_{on}/I_{off} \) ratio and small off-current overcame the key obstacle in graphene-based electronics.

Three terminal operation of GB offers various integrated device functionalities. Similar to the CMOS inverter operation, a series connection of n- and p-type complimentary GBs inverted the input signal \( V_{in} \) to its inverse \( V_{out} \) (Fig. 4C). The low \( V_{out} \) originated from the high on/off current ratio of GBs implying that only a small amount of static off-state power would be consumed. As for more complicated logic applications, we demonstrated a half-adder circuit built from n- and p-type 10 GBs, a remarkable result in high \( I_{on}/I_{off} \) ratio. We note that the large \( I_{on}/I_{off} \) ratio and small off-current overcame the key obstacle in graphene-based electronics.

In conclusion, our GB suggests the possibility of a graphene logic device by achieving a high on/off ratio of \( \sim 10^5 \), which exceeds the minimum requirement for logic transistors. Furthermore, the on/off ratio and the current density can be improved with well-developed semi-conductor processes since there is not a fundamental (or structural) limit. GB also has an advantage in lateral scaling as the barrier is formed vertically.

The absence of Fermi-level pinning, one of the major sources for high device resistance in silicon electronics, comes from the suppression of the surface states at the interface of silicon and graphene. In our GB, we could eliminate the “Fermi-level pinning” and manipulate the SB height as in the ideal Schottky-Mott limit (Fig. 3B), where the SB height is controlled through the selection of metal and semiconductor with appropriate WFs. Two different types of GB operations are possible, as shown in Fig. 4A. The first type uses the GB in the reverse-biased regime (orange shaded region in Fig. 4A). Here, a conventional FET-like device operation could be possible; i.e., the GB current, \( I \), had the tendency to saturate at large reverse bias voltages, and the “on” current, \( I_{on} \), had been modulated by \( V_{gate} \). The off state current, \( I_{off} \), was determined at the greatest attainable SB, which yielded an \( I_{on}/I_{off} \sim 300 \) in Fig. 4A. The second type of operation could be realized by using the device in the forward biasing region (the blue shaded region in Fig. 4A). In this regime, the GB current did not saturate as \( V_{bias} \) increased, but deviated from the typical FET-like device operation. However, near the diode turn-on regime, \( I \) varied by several orders of magnitude as \( V_{gate} \) changed, resulting in a switching operation with a large \( I_{on}/I_{off} \) ratio. Figure 4B shows the switching characteristic of the diode current in a forward biased p-type GB, demonstrating a remarkably high \( I_{on}/I_{off} \) ratio. We note that the large \( I_{on}/I_{off} \) ratio and small off-current overcame the key obstacle in graphene-based electronics.

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**Fig. 2.** Graphene barristor characteristics. The current and bias voltage characteristics of p-type (main panel) and n-type (inset) GBs at various fixed $V_{\text{gate}}$ values. $V_{\text{gate}}$ varies in the range -5 to 5 V with step size of 1 V for each curve. Red arrow indicates the direction of increasing $V_{\text{gate}}$.

**Fig. 3.** (A) Temperature dependent diode characteristic. The saturation current of the n-type GB, $I_{\text{sat}}$ is obtained by measuring the current at $V_{\text{bias}} = 2.5$ V at various temperature and gate voltage values. Different colors used for different $V_{\text{gate}}$ from -1V to 4V with 1~2 V step variation. The line fit for each $V_{\text{gate}}$ value is drawn to yield the Schottky barrier height from the slope of the fitted line. (B) The SB height obtained from the fit in (A) as a function of $V_{\text{gate}}$ (black squares, left axis). The graphene Fermi energy on the right axis is obtained from Hall measurement at the same gate voltage $V_{\text{gate}}$. Monotonic increase (decrease) of observed SB height consists with band diagram in Fig. 3C (3D). (C and D) Schematic band diagrams of GB with the electric field effect generated by the gate on the top of graphene. Applying negative voltage on the gate induces holes in graphene, increasing its work function and increasing the Schottky barrier height. As a result, the reverse current across the Schottky barrier decreases (C). Positive gate voltage decreases the Schottky barrier height and increases reversed current (D).
References and Notes


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Fig. 4. (A) Switching behavior of p-type GB in reverse (orange background) and forward (blue background) bias regimes. The GB current is plotted against the source drain bias at various fixed gate voltages. $V_{\text{gate}}$ varies in the range of -5 V - 5 V with a step of ~2 V. Black arrow indicates the direction of increasing $V_{\text{gate}}$. (B) The forward diode current as a function of gate $V_{\text{gate}}$ at fixed bias $V_{\text{bias}} = 0.3$ V. Unipolar control of forward current with the ratio of $10^5$ is obtained. (C) Inverter characteristics obtained from integrated n- and p-type GBs and schematic circuit diagram for the inverter. $V_{\text{DD}}$ is connected to p-type GB and the gain of the inverter is ~1.2. (D) Schematic of circuit design of a half-adder implemented with n- and p-type GBs. (E) Output voltage levels for SUM and CARRY for four typical input states.
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20. Materials and methods are available as supplementary materials on Science Online.

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References

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